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EXAMINER	
MARIAM, DANIEL G	
ART UNIT	**PAPER NUMBER**
2621	

DATE MAILED: 01/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/801,401	PINE, JOSHUA I.	
	Examiner	Art Unit	
	DANIEL G MARIAM	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. In response to the Office Action mailed on January 30, 2004, applicants have submitted an amendment filed on July 30, 2004, amending claim 11 and arguing to traverse the rejection of pending claims 1-22.

Response to Arguments

2. Applicants' arguments, see page 8 of the remarks, filed July 30, 2004, with respect to claims 11-13 and 16-17 have been fully considered and are persuasive. The 35 USC 102(e) rejection (Denton, et al) of claims 11-13 and 16-17 has been withdrawn.

3. With regard to the Telle reference, applicants argue starting on page 10 of the remarks, that Telle does not disclose an "image processing circuitry that is separate-and different-from its transformation circuitry so that it is possible to have an intermediate storage queue between the two". In response to applicants' argument that the reference fail to show certain features of applicants' invention, it is noted that the features upon which applicant relies (i.e., separate and different . . .) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicants further argue that Telle does not disclose an intermediate storage queue, communicatively coupled to the image processing circuitry, that stores one or more image data "awaiting additional processing by the imaging system. While the Examiner admits that Telle does not expressly store one or more image data awaiting additional processing by the *imaging system* (emphasis added), the reference to Schoenzeit, et al (5,619,624) does show this feature which will be discussed in the rejection below.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 11-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Konno, et al. (6,529,289).

With regard to claim 11, Konno, et al. discloses an electronic imager (Figs. 1 and 2), the electronic imager performing processing on an acquired image (See Figs. 1 & 2), the electronic imager comprising: a first and a second functional imaging subsystems, i.e., items 203 and 206 respectively, each imaging subsystem performing a processing, i.e., the formation of bit map data by the processors 203 and 206, step the acquired image (See Figure 1) the first imaging functional subsystem communicatively coupled to the second imaging functional subsystem and communicating to the second imaging functional subsystem an image data (as shown in Fig. 1); and an intermediate image storage buffer, i.e., items 204 and 207, communicatively coupled to the first and second imaging functional subsystems, the intermediate storage buffer storing one or more image data communicated from the first imaging functional subsystem to the second imaging functional subsystem (See for example, Fig. 1; and col. 19, lines 54-63).

With regard to claim 12, the electronic imager of claim 11, the first imaging subsystem comprising an image interface circuitry producing a raw image data (which correspond to item 74, in Fig. 2), the second imaging subsystem comprising an image processing circuitry that

processes the raw image from the image interface circuitry, and the intermediate image storage buffer storing one or more raw image data originating from the image interface circuitry (See Figures 1 and 2).

With regard to claim 13, the electronic imager of claim 12, wherein the one or more raw images are communicated to the intermediate storage buffer in response to a signal (See for example, item 74, in Fig. 2).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Telle (6,469,801) in view of Schoenzeit, et al. (5,619,624).

With regard to claim 1, Telle discloses an imaging system (See for example, Fig. 2) comprising: an image sensing circuitry that produces a raw image data (See item 50, in Fig. 2); an image processing circuitry, i.e., digital image processing, communicatively coupled to the image sensing circuitry, that processes the raw image data into a processed image data (See item 52, in Fig. 2); a transformation circuitry (which also corresponds to the digital image processing) communicatively coupled to the image processing circuitry, that transforms the processed image (the digital image processor does perform, among other things, a scaling operation, which generally is a transformation of an image from one size to another, such as enlarging or reducing) on the manipulated data into a final image data (See for example item 52, in Fig. 2;

and col. 5, lines 26-50); a communication circuitry, communicatively coupled to the transformation circuitry, that links the imaging system to a final storage (See for example, item 56, in Fig. 2; and item 30, in Fig. 2); an intermediate storage queue, i.e., buffer, communicatively coupled to the image processing circuitry, that stores one or more image data (See for example, item 60 and/or 56, in Fig. 2); and the intermediate storage queue storing one or more image data (awaiting additional processing by the imaging system) (See for example, col. 4, lines 12-34).

Telle does not expressly call for storing one or more image data awaiting additional processing by the imaging system. However, Schoenzeit, et al. (See for example, items 40a-40c; and col. 11, lines 11-14) teaches this feature. Therefore, it would have been obvious to one having ordinary skill I the art to incorporate the teaching as taught by Schoenzeit, et al. into the system of Telle if no other reason than to store image data or files awaiting additional processing by the system, and to do so would at least provide efficient storing and processing of a large amount of data in a timely manner.

With regard to claim 2, the imaging system of claim 1 wherein the intermediate storage queue is communicatively coupled to the image sensing circuitry and stores one or more raw image data, the one or more raw image data being delivered to the image processing circuitry upon the occurrence of an event (See item 60 and/or 54, in Fig.2).

With regard to claim 3, the imaging system of claim 2, wherein the one or more raw image data is held in the intermediate storage queue while the image processing circuitry is processing another image data, and one of the one or more raw image data is delivered to the image processing circuitry when the image processing circuitry ceases processing on the another

image data (See for example, image data provided by the user block item 30 to the digital image processor while the raw image data is stored in item 54 as illustrated in Fig. 2; and col. 8, lines 5-25).

With regard to claim 4, the imaging system of claim 2 wherein additional raw image data are stored in the intermediate storage queue, and each of the raw image data stored in the intermediate storage queue are delivered to the image processing circuitry when the amount of raw image data in the intermediate storage queue reaches a predetermined level (broadly reads on col. 4, line 43 through col. 5, line 19; particularly, col. 5, lines 14-19).

With regard to claim 5, the imaging system of claim 1 wherein the intermediate storage queue is communicatively coupled to the transformation circuitry and stores one or more processed image data, the processed image data being delivered to the transformation circuitry upon the occurrence of an event (See for example, item60, in Fig.2).

With regard to claim 6, the imaging system of claim 5 wherein the one or more processed image data is held in the intermediate storage queue while the transformation circuitry is processing another image data, and one of the one or more processed image data is delivered to the transformation circuitry when the transformation circuitry ceases processing on the another image data (See for example, item 60, in Fig.2).

With regard to claim 7, the imaging system of claim 5 wherein additional processed image data are stored in the intermediate storage queue, and each of the processed image data stored in the intermediate storage queue are delivered to the transformation circuitry when the amount of processed image data in the intermediate storage queue reaches a predetermined level (which broadly reads on col. 5, lines 14-19 and lines 26-50; and item 60, in Fig.2).

With regard to claim 8, the imaging system of claim 1 wherein the transformation circuitry performs a compression (this feature is also embedded in the digital image processor) on the image data (See for example, col. 4, lines 51-66).

With regard to claim 9, the imaging system of claim 1 further comprises a processing circuitry monitoring the status of the intermediate storage queue (See for example, item 46 or 60, in Fig. 2).

With regard to claim 10, the imaging system of claim 1, wherein the imaging system processes the image data in the intermediate storage queue in response to an indication that the imaging system has been linked to an external power source (See Fig. 2).

With regard to claim 11, an electronic imager the electronic imager performing processing on an acquired image (See for example, Fig. 2), the electronic imager comprising: a first and a second functional imaging subsystems, i.e., items 50 and 52 respectively, each imaging subsystem performing a processing step the acquired image (as shown in Fig. 2), the first imaging functional subsystem communicatively coupled to the second imaging functional subsystem and communicating to the second imaging functional subsystem an image data (See item 50 which clearly is coupled to item 60, in Fig. 2); and an intermediate image storage buffer, i.e., item 60 and/or 54, communicatively coupled to the first and second imaging functional subsystems, the intermediate storage buffer storing one or more image data communicated from the first imaging functional subsystem to the second imaging functional subsystem (See for example, Fig. 2).

With regard to claim 12, the electronic imager of claim 11, the first imaging subsystem comprising an image interface circuitry producing a raw image data, the second imaging

subsystem comprising an image processing circuitry that processes the raw image from the image interface circuitry, and the intermediate image storage buffer storing one or more raw image data originating from the image interface circuitry (See for example, item 30 and/or items 36, 50; and item 60, in Fig. 2).

With regard to claim 13, the electronic imager of claim 12, wherein the one or more raw images are communicated to the intermediate storage buffer in response to a signal (See for example, Fig. 2).

With regard to claim 14, the electronic imager of claim 13 wherein the signal indicates that the image interface circuitry is producing a raw image at a faster rate than the processing circuitry can process the raw image (it is obvious that the raw image generator has only one function, that is, to generate a raw image while the processor does various processes, such as scaling manipulation, compression, etc., and thus the time taken by the processor is longer than the raw image generator, See Fig. 2).

With regard to claim 15, the electronic imager of claim 13 wherein the signal indicates that the intermediate storage buffer contains less than a predetermined amount of raw image data (which reads on the various modification or alteration performed on the raw image data, including scaling and compression; See for example, Figs. 2 and 7).

With regard to claim 16, the electronic imager of claim 11, the first imaging subsystem comprising an image processing circuitry producing a processed image data, the second imaging subsystem comprising a transformation circuitry that processes the processed image from

the image processing circuitry (which reads on item 60, in Fig. 2), and the intermediate image storage buffer storing one or more processed image data originating from the image processing circuitry (item 56, in Fig. 2).

With regard to claim 17, the electronic imager of claim 16, wherein the one or more processed images are communicated to the intermediate storage buffer in response to a signal (See items 52 and 56, in Fig. 2).

With regard to claim 18, the electronic imager of claim 17 wherein the signal indicates that the image processing circuitry is producing a processed image at a faster rate than the transformation circuitry can process the processed image (which does read on item 52, in Fig.2, since both image processing and scaling, i.e., transformation, are performed by the same digital image processing, item 52, in Fig. 2).

With regard to claim 19, the electronic imager of claim 17 wherein the signal indicates that the intermediate storage buffer contains less than a predetermined amount of processed image data (which reads on the various modification or alteration performed on the raw image data, including scaling and compression; See for example, Figs. 2 and 7).

With regard to claim 20, a method of operating an imaging system, the imaging system comprising an image sensor, an interface circuitry, and an image processing circuitry (See for example, Fig. 2), the method comprising the steps of, acquiring an initial image in the image sensor (See for example, item 50, in Fig. 2); producing a first image data from the initial image in the interface circuitry (See for example item 54, in Fig. 2); processing the first image data into a second image data (See for example, item 52, in Fig. 2); and selectively storing the first image data in a buffer based on whether the step of processing is already operating on a previously

communicated first image data (see for example, item 60, in Fig. 2; col. 4, lines 12-34; and col. 8, lines 5-25).

With regard to claim 21, the method of claim 20 wherein the step of processing the first image data into a second image data further comprises the step of transforming a processed image data into a final image data in a transformation circuitry (which also corresponds to item 52, in Fig. 2), and the step of selectively storing comprises storing the processed image (item 56, in Fig. 2).

With regard to claim 22, the method of claim 20 wherein the step of processing the first image data into a second image data further comprises the step of transforming a raw image data into a processed image data in an image processing circuitry (See item 52, in Fig. 2), and the step of selectively storing comprises storing the raw image (See for example, item 60, in Fig. 2).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL G MARIAM whose telephone number is 703-305-4010. The examiner can normally be reached on M-F (7:00-4:30) FIRST FRIDAY OFF.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, LEO BOUDREAU can be reached on 703-305-4607. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DANIEL MIRIAM
PRIMARY EXAMINER

January 10, 2005